In the Specification:

Please substitute the following paragraphs for the corresponding paragraphs beginning at the indicated location in the specification as originally filed.

Page 8, line 20+:

FIG. 11 shows etching off the oxide 14a and 70a on the NFET only while etching the nitride layer off of all regions, including nitride spacer ~~15a and 15b~~ 14a and 14b and the buffer nitride ~~10a and 10b~~ 11a and 11b on top of the gate poly. N-extension 120 is performed, preferably with arsenic implantation through the notch 110 formed as a result of nitride spacer ~~15a~~ 14a removal. See FIG. 12.